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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/800,764	03/06/2001	Aki Korhonen	019703000410	3899

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	5

DATE MAILED: 03/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/800,764	Applicant(s) KORHONEN, AKI	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because the data paths 105 and 107 are not properly shown. It is not clear graphically if the data in the access paths are transmitted directly from the Bus/memory interface 110 to the CPU core 104, or indirectly through cache 106 and 108.

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

This application lacks formal drawings because of the hand written legends. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-14, 22 and 23 are rejected under 35 U.S.C. 101 because the disclosed invention is inoperative and therefore lacks utility.

The claimed feature of "loading a test program code into an area of the system memory to be tested, ... configured to detect one or more defects in the system memory", recited in the independent claims 1, 12, 22 and 23, renders the claimed invention inoperable and therefore lacking utility. The test program, which is loaded into an area of the system memory for detecting defects in such memory, is not capable of verifying the condition of the memory, since the test program, which resides in the same memory area under test, cannot function properly if the memory area is initially defective.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-14, 22 and 23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not clearly describe the claimed subject matter of "loading a test program code into an area of the system memory to be tested" and detecting in the system memory where the test program is loaded, as recited in the

independent claims 1, 12, 22 and 23, so as to enable one skilled in the art to make and or use the invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 12-14 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 12 and 23 are hybrid claims, because claim 12 includes the limitation of one "instruction" in an apparatus and claim 23 included the limitations of "program code" and "instruction" in a system without specifying the means associated with the function, for example such as storage means where a test program code with instructions is normally stored.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the

United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 and 12-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Cepulis et al. (US 6463550), ISSUED: October 8, 2002 and FILED: March 12, 1999.

Regarding Claims 1, 12, 15, 20, 22 and 23, Cepulis discloses a method and apparatus for implementing a suitable fault detection scheme to test various devices, shown in (FIG. 1, computer system 100) including one or more central processing units (CPUs 102) and a system memory array 118 including memory modules 112, configurable to replace defective portions, comprising:

Loading a test program code, such as the BIOS code from the BIOS ROM 122 into an area of the system memory array 118 to be tested having a plurality of instructions configured to detect one or more defects in the system memory, fetching an instruction of the test program code from the system memory 118 and executing the fetched instruction within a CPU 0, during the boot-up process, generally referred to as "power on self test" (POST), which are part of the Basic Input Output System (BIOS) code that is stored in read-only memory (ROM) and executed by the CPU 0.

Determining whether the executed instruction yields a test result in conformance with an expected result, where the computer system 100 implements a suitable fault detection scheme to test various devices, such as the CPU 102 and memory modules 112, for determining whether a device has failed during POST or during normal system operation. If a match does not exist, between the write and read data, then the memory is deemed defective, otherwise, the device is assumed to be functional. A CPU

typically includes logic to test itself, where the BIOS code reads the contents of various status registers internal to the CPU that indicate the CPU's functional state.

Regarding Claims 2, 3, 13, 14, 16-19 and 21, Cepulis discloses reporting the test result in the NVRAM 130, which includes a Failed Device Log (FDL) 132 having a list of those components in the computer system 100 that have been tagged as failed. If a device is determined to be defective, one of the CPU's 102 places an entry into the FDL 132 identifying that physical device as failed. Also, removing a CPU upon the BIOS code determining that a CPU is defective in FDL 132, the user may replace the defective CPU with a new CPU, and further de-allocating a portion of the system memory if a memory device has failed in FDL 132, the user may wish to replace the defective memory device or simply add additional memory modules without removing the defective device, FIGS. 1 and 3.

Regarding Claim 4, Cepulis discloses determining the area of the system memory array 118 including memory modules 112 to be tested, generating the test program code in BIOS ROM 122 and loading the operating system into the computer's main system memory array 118, designed to detect the one or more defects and simulating execution of the test program code BIOS ROM 122 by assigning faults to generate the expected result, FIG. 1.

Regarding Claim 5, Cepulis discloses switching a CPU to protect mode, changing a segment limit of the CPU and switching the CPU to big real mode, as shown in FIG. 1. The CPU's 102 are designated as (CPU 0, CPU 1, CPU 2, and CPU N), where the North bridge device 106 facilitates the transfer of data and commands

between devices connected to the CPU, memory, and PCI buses 110, 114, and 108, and permits the CPU 102 to communicate with the I2 C master 140.

Regarding Claim 6, Cepulis discloses before executing the fetched instruction installing an exception handler to branch a flow of CPU program control upon detection of a defect, disabling the interrupts to prevent interruption in the execution of the test program code, after executing the instruction, enabling the interrupts, and removing the exception handler. If a component failure occurs during normal operation (block 304), then an interrupt signal is transmitted to a CPU 102 (block 308), indicating a severe problem within the computer system 100, which typically suspends execution of the operating system software. The program is known as an interrupt, which is stored in the memory array 112 or the BIOS ROM.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cepulis et al. (US 6463550).

Regarding Claims 7-11, Cepulis does not explicitly perform a direct measurement of CPU clock cycles in seconds and comparing the measured test result against an expected number. However, he discloses self testing of the CPU, which typically includes logic to test itself, where the BIOS code reads the contents of various status registers internal to the CPU that indicate the CPU's functional state. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use the self- test logic in the device and method of Cepulis for the purpose of measuring the CPU execution timing, so as to enhance the test fault detection and isolation performance for the computer system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James C Kerveros
Examiner
Art Unit 2133

By: _____.

U.S. PATENT OFFICE
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Date: 2/25/04
Non-Final Rejection

Guy J. Lamarre
for

Albert DeCady
Primary Examiner